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## FOREWORD

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### Special Section on VLSI Design and CAD Algorithms

In the past decades, semiconductor key devices have been contributed for IT, ICT, and IoT technologies and industries which realized human relationships. From now on, Industrial Internet of Things (IIoT) is possible to create a new world such as health and wellness environment in the post-pandemic era. In order to realize and accelerate the vision, VLSI technology and CAD algorithms is one of the important supporting technologies for Digital Twin, artificial intelligence and data assimilation. Hopefully this series of special sections helps researchers to acquire cutting-edge of work on VLSI design and CAD algorithms.

In this special section, we have received 16 papers. We made thorough reviews, had online paper selection meetings of all editorial committee members, and finally selected 8 papers. These papers are categorized into 5 topics: 1) Device and Circuit Modeling and Analysis, 2) Circuit Design, 3) Physical Level Design, 4) Logic Synthesis, Test and Verification and 5) High-Level Synthesis and System-Level Design. They cover a wide variety of research areas.

On behalf of the guest editorial committee, I would like to express our sincere appreciation to all authors of papers submitted to this special section. I would also like to express my thanks to all members of the guest editorial committee and all reviewers for their work on selecting papers. I should thank Prof. Shimpei Sato, Tokyo Institute of Technology and Prof. Hiroyuki Tomiyama, Ritsumeikan University for their work as Guest Editors. Thanks are also due to the IEICE headquarters for the support to this special section.

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Noriyuki Minegishi, Guest Editor-in-Chief

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**Noriyuki Minegishi** (*Member*) received a Ph.D in Electrical Engineering and Computer Science from Kanazawa University in 2005. He joined Mitsubishi Electric Corporation in 1985, where he is a currently a chief researcher. His research interests include data analysis and optimization, data assimilation, prognostics health management, formal methods design and IIoT architecture. He was Chair of VLSI Design, IEICE. He is a visiting professor of Kanazawa University since 2014.

